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1 Analog design space exploration: Efficient description of the design space of analog circuits

Maria del Mar Hershenson

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(140.90 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present a method for determining the feasible set of analog design problems and we propose an efficient method for their verification. The verification method presented relies on the formulation of the analog circuit design problem as a convex optimization problem in both the design variables and the performance specifications. Since the design is convex not only in the design variables but also in the specification parameters, we observe that the feasible sets are convex and po ...

Keywords: analog, circuits, convex programming, geometric program, optimization, synthesis, verification

2 GENAC: an automatic cell synthesis tool

C.-L. Ong, J.-T. Li, C.-Y. Lo

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**

Full text available: pdf(628.21 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a solution to the layout problem of cell synthesis, which achieves multiple optimization objectives. In particular, we propose a new hierarchical method for fast and optimal placement of the transistors in a cell. The method minimizes the number of diffusion breaks, and allows a further pursuit of a secondary optimization objective, such as routing channel density. For cells with non-uniform transistor widths, the transistors are folded in such a way as to optimize a cost functio ...

3 Cell map representation for hierarchical layout

J. Soukup, J. Royle

June 1980 **Proceedings of the 17th conference on Design automation**

Full text available: pdf(330.69 KB) Additional Information: full citation, abstract, references, citings, index terms

In the hierarchical layout of rectangular blocks, the routing area naturally breaks into a set of adjacent rectangles. These rectangles can be used as basis for both loose routing and the

final track assignment. The paper explores some ways of structuring the required data. More details about generalized Lee routing, and practical results are left for verbal presentation.

4 CELLERITY: a fully automatic layout synthesis system for standard cell libraries

Mohan Guruswamy, Robert L. Maziasz, Daniel Dulitz, Srilata Raman, Venkat Chiluvuri, Andrea Fernandez, Larry G. Jones

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(104.51 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper describes a fully automatic standard-cell layoutsynthesis system, CELLERITY. The system is flexible insupporting a wide variety of process technologies and a range oflibrary template styles. The tool is fully automatic and providesseveral options to the user to customize the layout template. Thetool considers performance and yield and generates dense,design-rule correct layouts. Experimental results indicate that thearea of CELLERITY-generated standard cells is competitive withmanuall ...

5 Clustering based simulated annealing for standard cell placement

Sivanarayana Mallela, Lov K. Grover

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available: pdf(619.83 KB) Additional Information: full citation, abstract, references, citings, index terms

Simulated annealing has been shown to be effective in producing good quality results for the standard cell placement problem. Its main drawback is the excessive computation time required, which increases significantly with the problem size. In this paper we present a novel technique for reducing the effective problem size for simulated annealing without compromising the solution quality. We form clusters of cells based on their interconnections, and place t ...

6 Accurate and efficient fault simulation of realistic CMOS network breaks

Haluk Konuk, F. Joel Ferguson, Tracy Larrabee

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(260.64 KB) Additional Information: full citation, references, index terms

7 A global routing algorithm for general cells

Gary W. Clow

June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(554.39 KB) Additional Information: full citation, abstract, references, citings, index terms

An algorithm is presented which accomplishes the global routing for a building block or general cell routing problem. A line search technique is employed and therefore no grid is assumed either for the module placements or the pin locations. Instead of breaking the routing surface up into channels, a maze search finds acceptable global routes while avoiding the blocks. Both multi-pin terminals and multi-terminal nets are accomodated. It is shown that the Lee-Moore grid-based appr ...

8 Advances in SAT: Solving difficult SAT instances in the presence of symmetry

Fadi A. Aloul, Arathi Ramani, Igor L. Markov, Karem A. Sakallah

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(378.79 KB) Additional Information: full citation, abstract, references, citings, index terms

Research in algorithms for Boolean satisfiability and their implementations [23, 6] has recently outpaced benchmarking efforts. Most of the classic DIMACS benchmarks [10] can be solved in seconds on commodity PCs. More recent benchmarks take longer to solve because of their large size, but are still solved in minutes [25]. Yet, small and difficult SAT instances must exist because Boolean satisfiability is NP-complete.We propose an improved construction of symmetry-breaking clauses [9] and apply ...

Keywords: CNF, SAT, difficult, faster, instances, search, speed-up, symmetry

9 A fully automatic hierarchical compactor

George Entenman, Stephen W. Daniel
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(922.86 KB) Additional Information: full citation, abstract, references, citings, index terms

A fully automatic hierarchical compactor has been developed to translate hierarchical, symbolic cell designs into artwork. The hierarchical compactor takes advantage of the fact that a typical hierarchical design uses the same cell in several different places. Each cell is first examined in all of its contexts. The leaf-cell compactor next compacts each leaf-cell to its minimum possible size in its worst-case environment. The last step is to abut instances of the cells according to ...

10 A unified approach to the extraction of realistic multiple bridging and break faults

Gerald Spiegel, Albrecht P. Stroele
December 1995 **Proceedings of the conference on European design automation**

Full text available: pdf(654.87 KB) Additional Information: full citation, references, citings, index terms

11 Transistor level micro-placement and routing for two-dimensional digital VLSI cell synthesis

Michael A. Riepe, Karem A. Sakallah
April 1999 **Proceedings of the 1999 international symposium on Physical design**

Full text available: pdf(1.29 MB) Additional Information: full citation, references, citings, index terms

12 An efficient layout style for 2-metal CMOS leaf cells and their automatic generation

Chi-Yi Hwang, Yung-Ching Hsieh, Youn-Long Lin, Yu-Chin Hsu
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(750.81 KB) Additional Information: full citation, references, citings, index terms

13 Retargeting of mixed-signal blocks for SoCs

R. Castro-López, F. Fernández, M. Delgado-Restituto, A. Rodriguez-Vázquez
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(49.96 KB) Additional Information: full citation, references, index terms

14 Timing issues in placement: Modeling repeaters explicitly within analytical placement

Prashant Saxena, Bill Halpin
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(699.52 KB) Additional Information: full citation, abstract, references, index terms

Recent works have shown that scaling causes the number of repeaters to grow rapidly. We demonstrate that this growth leads to massive placement perturbations that break the convergence of today's interleaved placement and repeater insertion flows. We then present two new force models for repeaters targeted towards analytical placement algorithms. Our experiments demonstrate the effectiveness of our repeater modeling technique in preserving placement convergence (often also accompanied by wire-le ...

Keywords: analytical placement, buffering, force-directed placement, interconnect, placement, repeater insertion, scaling

15 Cell-based hierarchical pitchmatching compaction using minimal LP
So-Zen Yao, Chung-Kung Cheng, Debaprosad Dutt, Surendra Nahar, Chi-Yuan Lo
July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available: pdf(531.59 KB) Additional Information: full citation, references, index terms

16 CLIP: integer-programming-based optimal layout synthesis of 2D CMOS cells
Avaneendra Gupta, John P. Hayes
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(371.02 KB) Additional Information: full citation, abstract, references, index terms

A novel technique, CLIP, is presented for the automatic generation of optimal layouts of CMOS cells in the two-dimensional (2D) style. CLIP is based on integer-linear programming (ILP) and solves both the width and height minimization problems for 2D cells. Width minimization is formulated in a precise form that combines all factors influencing the 2D cell width—transistor placement, diffusion sharing, and vertical in ...

Keywords: CMOS networks, circuit clustering, diffusion sharing, integer linear programming, integer programming, layout optimization, leaf cell synthesis, module generation, transistor chains, two-dimensional layout

17 Global routing considerations in a cell synthesis system
Dwight Hill, Don Shugard
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(601.41 KB) Additional Information: full citation, abstract, references, citings, index terms

Cell synthesis is the process of turning a netlist into an efficient layout without being restricted to a library of predesigned cells or a fixed floorplan. Normally, this job is broken into at least three parts: placement, routing, and detailed cell generation. Each of these tasks are often divided further into a global and a detailed phase. This paper presents cell synthesis system called Sea Of Devices (SOD), with emphasis on its routing phase. In particular, SOD uses a new model for the ...

18 Coping with buffering: Diffusion-based placement migration
Haoxing Ren, David Z. Pan, Charles J. Alpert, Paul Villarrubia
June 2005 **Proceedings of the 42nd annual conference on Design automation**

Full text available: pdf(772.26 KB) Additional Information: full citation, abstract, references, index terms

Placement migration is the movement of cells within an existing placement to address a variety of post-placement design closure issues, such as timing, routing congestion, signal integrity, and heat distribution. To fix a design problem, one would like to perturb the design as little as possible while preserving the integrity of the original placement. This work presents a new diffusion-based placement method based on a discrete approximation to a closedform solution of the continuous diffusion ...

Keywords: diffusion, legalization, placement migration

19 TimberWolf3.2: a new standard cell placement and global routing package

Carl Sechen, Alberto Sangiovanni-Vincentelli

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, citings, index terms

TimberWolf3.2 is a new standard cell placement and global routing package. The placement and global routing proceed over 3 distinct stages. The general combinatorial optimization technique known as simulated annealing is used during the first two stages of the placement. In the first stage, TimberWolf3.2 places the cells such that the total estimated interconnect cost is minimized. During the second stage, TimberWolf3.2 inserts feed through cells as required and the minimization of the tota ...

20 An over-cell gate array channel router

Howard E. Krohn

June 1983 **Proceedings of the 20th conference on Design automation**

Full text available: pdf(425.28 KB) Additional Information: full citation, abstract, references, citings, index terms

A gate array router that utilizes horizontal and vertical over-cell routing channels to increase cell density is described. Logic macros, with fixed intraconnect metal that may span several cell columns, are mapped onto the array producing partially filled routing channels. Macro interconnects are loosely assigned to the partially filled horizontal and vertical routing channels during global routing. Each loose horizontal channel segment is assigned to a channel track using a maze router. V ...

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IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. **A new optimization driven clustering algorithm for large circuits**
Ding, C.-L.; Ho, C.-Y.; Irwin, M.J.;
Design Automation Conference, 1993, with EURO-VHDL '93. Proceedings EUI European
20-24 Sept. 1993 Page(s):28 - 32
Digital Object Identifier 10.1109/EURDAC.1993.410612
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